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EXAMINER	
KIELIN, ERIK J	

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2813	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/943,078	Applicant(s) ABBOTT, TODD R.	
	Examiner Erik Kielin	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,14-16,39 and 45-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,14-16,39 and 45-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This action responds to the amendment filed 7 January 2003.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, steps in the formation of the gate area and the local interconnect area in the same trench (instant claims 1 and 39) and), the steps in the formation of the isolation region (instant claim 4), must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-11, 14-16, 39 and 45-49 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for forming a gate structure and an interconnect structure in *separate* trenches, does not reasonably provide enablement for forming a gate structure and an interconnect structure in the *same* trench. The specification does not enable any

person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims.

Regarding independent claims 1 and 39, the drawings and the specification make it clear that the gate and the interconnect structures are formed in separate trenches 44 and 46, respectively. (See especially Fig. 10 and p. 11, second paragraph, which indicates that the gate and interconnect are formed in separate trenches 44 and 46, respectively and not in the same or a single trench.)

While Examiner acknowledges that the instant specification at page 15, lines 15-27, referring to Fig. 16, states in pertinent part,

> "The first and second strips 268, 274, and wordline 255 form conductive interconnects and may be fabricated as a damascene trenches as discussed with reference to Figs. 1-13."

But Figs. 1-13 cannot be used to form the strips shown in Fig. 16 because, as shown in Figs. 1-13, the gate and interconnect structures are formed in *separate* trenches 44 and 46, which are specifically polished down to "the dielectric layer" 40 (Figs. 8 to 9A) and then coated with other dielectric layers 104, 106 (Fig. 13). As such there can be no overlying conductive material in the strip regions 268, 274 of Fig. 16 that is not specifically in the separate trenches in which the gate (e.g. 214, 222) and interconnect structures (e.g. 270, 272) have been formed, by the method of that shown in Figs. 1-13. Accordingly, the instant specification does not enable the formation of that shown in Fig. 16 by the method which the specification states that the structure in Fig. 16 may be fabricated --namely that shown in Figs. 1-13.

The remaining claims are not enabled for depending from the independent claim 1.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 5, 6, 8, 10, 46, 47, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 3,891,190 (**Vadasz**) in view of US 6,037,248 (**Ahn**).

Regarding claims 1 and 10, **Vadasz** discloses a method of fabricating a semiconductor device comprising:

forming a first dielectric layer **12** (Fig. 1a) over a base substrate **10** (Fig. 1a; col. 3, lines 3-16);

forming a damascene trench **14** in said first dielectric layer **12**, said trench having a gate area and a local interconnect area (Figs. 1b-1c);

forming a gate oxide layer **20** (Fig. 1b) on said base substrate **10** within said gate area of said damascene trench 14 (Fig. 1b-1c; col. 3, lines 61-68);

filling said damascene trench **14** with a conductive material **24** which is polysilicon --as further limited by instant claim 10 (col. 4, lines 15-17; Fig. 1d-1e);

defining a damascene gate structure **20, 36** and a damascene local interconnect structure **38, 40** (Fig. 1e-1f; col. 8, lines 40-45).

Vadasz does not teach removing the first dielectric layer **12**.

Ahn teaches the benefits of removing the first dielectric layer to have an air dielectric **56** around the gate structure **33**, **36**, **37** and the interconnect structure **48**, **53**, **54**, **72**, **etcetera** to reduce the capacitance and the RC delay associated therewith (Abstract; col. 5, lines 43-46).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to remove the dielectric layer of **Vadasz**, as taught by **Ahn** to reduce RC delay.

Regarding claim 5, **Vadasz** shows the first dielectric layer **12** to be conformal over the substrate **10**.

Regarding claim 6, the damascene trench is formed by forming a patterned mask over the first dielectric layer **12**, etching through the dielectric layer to the base substrate **10** in areas defined by said patterned mask; and stripping said patterned mask (col. 3, lines 2-40).

Regarding claim 8, **Vadasz** discloses that the formation of the gate oxide 20 comprises:

growing an oxide layer **20** on said base substrate **10** (Fig. 1b);

forming a patterned mask over said semiconductor device, said pattern arranged to expose at least a portion of said oxide layer **20** within said local interconnect area;

etching away the exposed portion of said oxide layer (Fig. 1c); and

stripping said patterned mask from said semiconductor device (col. 3, lines 62-68).

Regarding claims 46 and 47, although **Vadasz** does not show a plurality of gate and interconnect areas in said damascene trenches, it would have been obvious for one of ordinary skill in the art, at the time of the invention to form plural such areas in order to form a higher density of structures on the substrate and thereby a faster device. The courts have held that mere duplication of parts has no patentable significance unless a new or unexpected result is produced

see *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). In the instant case, there is no evidence of unexpected results.

Regarding claim 49, **Vadasz** discloses that the gate and interconnect areas of the damascene trench **14** are formed with said patterned mask and etching.

6. Claims 7, 9, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Vadasz** in view of **Ahn** as applied to claims 1 and 8 above, and further in view of **Wolf**, et al. Silicon Processing for the VLSI Era, Vol. 1-Process Technology, Lattice Press: Sunset Beach CA, 1986, pp. 280-282, 397-399.

Regarding claims 7 and 9, **Vadasz** forms a diffused regions **48**, **50** (source/drain regions) in the base substrate **10** in the damascene trench (Fig. 1f), but does not indicate that method is by implantation or that implantation occurs prior to removal of the patterned mask used to form the damascene trench.

Wolf teaches the benefits of implantation with an entire page of advantages (p. 282) which are incorporated herein.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to form the implant of **Vadasz** by the method of **Wolf** for the numerous benefits indicated therein.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to leave the patterned mask in place during the implantation to protect the dielectric layer from being implanted with impurities and also to prevent penetration through the dielectric layer into the substrate yielding undesired implantation regions. Moreover, it has been held that the

selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results. See *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946). No unexpected results are presently of record for this process order.

Regarding claim 11, **Vadasz** does not teach the formation of a silicide over the gate region, but **Wolf** teaches that silicide formation over the gate region reduces contact resistance (pp. 397-399).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to form a silicide over the gate region of **Vadasz** to reduce contact resistance, as taught by **Wolf**.

7. Claims 1-3, 15, 45, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,083,827 (**Lin** et al.) in view of **Ahn**.

Lin discloses a method of fabricating a semiconductor device comprising:

forming a first dielectric layer **228** over a base substrate **200** (Fig. 2A);

forming a damascene trench **232** in said first dielectric layer **228**, said trench having a gate area and a local interconnect area (Fig. 2C-2D);

forming a gate oxide layer **210** (Fig. 1b) on said base substrate **200** within said gate area of said damascene trench **232** (Figs. 2D);

filling said damascene trench **232** with a conductive material **240** (Fig. 2D);

defining a damascene gate structure **210, 214** and a damascene local interconnect structure **240b** (Fig. 2E).

Lin does not teach removing the first dielectric layer **228**.

Ahn teaches the benefits of removing the first dielectric layer to have an air dielectric **56** around the gate structure **33**, **36**, **37** and the interconnect structure **48**, **53**, **54**, **72**, **etcetera** to reduce the capacitance and the RC delay associated therewith (Abstract; col. 5, lines 43-46).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to remove the dielectric layer of **Lin**, as taught by **Ahn** to reduce RC delay.

Regarding claims 2 and 48, **Lin** forms shallow trench isolations **202** in the base substrate before the formation of first dielectric layer **228** (Fig. 2A; col. 2, lines 56-57).

Regarding claim 3, **Lin** shown a portion of the damascene trench **232** overlies the isolation trench **202** as shown in Fig. 2C.

Regarding claim 15, **Lin** shows spacers **220** next to the gate and interconnect structures (Figs. 2D-2E).

Regarding claim 45, **Lin** shows the local interconnect 240b overlies the isolation trench 202, as shown in Figs. 2D and 2E.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Lin** in view of **Wolf**, Silicon Processing for the VLSI Era, Vol. 2-Process Integration, Lattice Press: Sunset Beach CA, 1990, pp. 20-22, 39-41.

The prior art of **Lin**, as explained above, discloses each of the claimed features except for all of the details in the formation of the isolation trenches **202.**

Wolf teaches a conventional method to form isolation trenches comprising,

depositing a pad oxide layer over the base substrate (Fig. 2-26);

depositing a nitride layer over the pad oxide layer;

forming a mask over said nitride layer;

etching through portions of said nitride layer and said pad oxide layer and into said substrate defining an isolation trench opening in the substrate;

stripping away the mask; and filling the isolation trench opening with a dielectric material; and

removing the pad oxide and nitride.

(See pp. 39-41 for the general process --especially Fig. 2-26. Note that Wolf indicates that the pad oxide and nitride are etched as in the conventional LOCOS process which is discussed on pp. 20-22 especially at p. 21, section entitled "2.2.2.3 Mask and Etch Pad-Oxide/Nitride Layer to Define Active Regions.")

It would have been obvious for one of ordinary skill in the art, at the time of the invention to form the isolation trenches of **Lin** by the method in **Wolf** because **Lin** is silent to the method such that one of ordinary skill would use well known methods of forming an isolation region, such as that taught in **Wolf**.

Allowable Subject Matter

9. The following is a statement of reasons for the indication of allowable subject matter:

Although claims 14, 16, and 39 stand rejected under 35 USC 112(1), the claims are believed to have allowable subject matter should Applicant overcome the rejection under 35 USC 112(1).

Regarding independent claim 39, the prior art of **Vadasz**, **Lin** and **Ahn**, teaches each of the limitations of the claims but would not be properly combined. For example, although **Lin**

teaches a planarization step as require in instant claim 39, such planarization would frustrate the invention of **Vadasz** who forms and leaves interconnect over the dielectric layer.

Regarding claims 14 and 16, the applied art does not teach or suggest in proper combination with the other claimed features, that the lightly-doped drain regions are formed *after* the removal of the dielectric layer. Such would be at best obvious to try in the applied references.

Response to Amendment

10. Cancellation of claims 12 and 13 is acknowledged.

In light of the amendment of the claims to include the limitation that the interconnect structure "form[s] a connection to said base substrate" in independent claim 1, all prior art rejections over the Chen reference have been withdrawn because Chen does not teach this limitation.

The objection to the specification has been withdrawn in light of the amendments to the specification.

Response to Arguments

11. Applicant's arguments with respect to the prior art rejections of claims 1-16 and 39 have been considered but are moot in view of the new ground(s) of rejection.

12. Applicant's arguments filed 7 January 2003 regarding the objection to the drawings and the rejection of the claims under 35 USC 112(1) have been fully considered but they are not persuasive.

Regarding the drawings, Applicant argues that Fig. 16 shows both interconnect structures (e.g. 270, 272) and gate structures (e.g. 214, 222) formed in the same damascene trenches (e.g. 268, 274). This is not a showing of the claimed steps which are presently shown in Figs. 1-13 which show formation of the gate and interconnect structures in separate trenches -- not the same trench. Moreover, because the passage in the specification to which Applicant refers (page 15, lines 15-27) does not enable the formation of the structure shown in Fig. 16 for reasons already indicated in the rejection of the claims under 35 USC 112(1) and incorporated herein in their entirety, there remains no showing of the claimed subject matter.

In regard to the lack of showing of the steps of claim 4 of forming the isolation region, Applicant argues that the steps are not essential for the understanding of the invention. Examiner respectfully disagrees. Inasmuch as Applicant has provided such details in a claim, they are critical to an understanding of the invention. Furthermore, the rectangular box in Fig. 14 does not show the steps. Accordingly the claimed subject matter is not shown and the objection has been maintained.

Regarding the rejection of the claims under 35 USC 112(1), scope of enablement, Applicant argues, that the specification is enabling for the formation of the gates and interconnect structures in a single trench simply because it is mentioned in the specification and presumptively shown in Fig. 16 that this can be done. Examiner respectfully disagrees for the reasons indicated in the rejection of the claims under 35 USC 112(1), above, which rejection is incorporated herein by reference. In particular, because the specification contradicts itself with regard to the statement that the structure shown in Fig. 16 could be formed by the method shown is Figs. 1-13, which clearly show that the gate and interconnect structures are formed in separate

trenches, one of ordinary skill would have no way of knowing how to form them in the same trench by the method shown in Figs. 1-13 and discussed in the specification.

In short, a mere statement that something may be done does not necessarily enable the means to do said something. In light of the contradictory showings between Figs. 1-13 and Fig. 16, lack of enablement is further supported by Applicant's own specification.

Conclusion

This action is made non-final to allow Applicant to respond to the new ground of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 703-306-5980. The examiner can normally be reached on 9:00 - 19:30 on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Erik Kielin
February 4, 2003